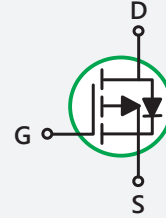
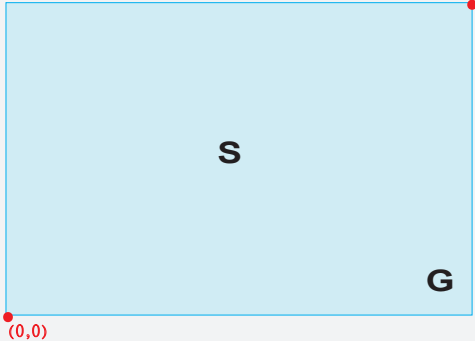


-100V P Channel Enhancement MOSFET Wafer Datasheet

FEATURES

- P-Channel, -100V
- $R_{ds(ON)} = 183m\Omega$ (Typ.) @ $V_{GS} = -10V$
- Exceptional on-resistance and maximum DC current capability
high density cell design for extremely low $R_{DS(ON)}$



Bonding Pad Information	Chip Information	
	Wafer Name	DC6M100P183M7
	Wafer Diameter	6 inches
	Wafer Thickness	7 mils
	Front-side Metallization	Al/Si/Cu (4um)
	Back-side Metallization	Ti/Ni/Ag
	Bonding Type	Gate: 1.5mil Cu x 1
		Source: 1.5mil Cu x 8
	Die Size (without scribe line)	1440um x 1000um
	Scribe Line Width	60um
	Gate Pad Size	180um x 180um
Gross Die	10K ea	

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80V, V_{GS} = 0V$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.6	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -1A$		183	225	m ohm
		$V_{GS} = -4.5V, I_D = -1A$		205	256	m ohm

Notes:

1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
2. $R_{DS(ON)}$ calculated by SOP-8 Package Type.