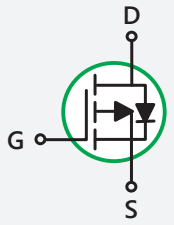
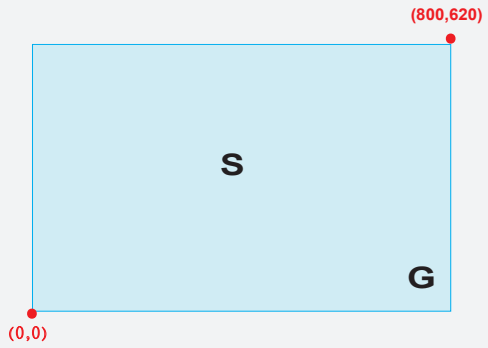
-100V P Channel Enhancement MOSFET Wafer Datasheet

FEATURES

- P-Channel,-100V
- Rds(ON)= 645mΩ (Typ.)@VGS=-10V
- Exceptional on-resistance and maximum DC current capability high density cell design for extremely low RDS(ON)



Bonding Pad Information	Chip Information	
	Wafer Name	DC6M100P645M7
	Wafer Diameter	6 inches
	Wafer Thickness	7 mils
	Front-side Metallization	Al/Si/Cu (4um)
	Back-side Metallization	Ti/Ni/Ag
	Bonding Type	Gate: 1.5mil Cu x 1
		Source: 1.5mil Cu x 5
	Die Size (without scribe line)	800um x 620um
	Scribe Line Width	60um
	Gate Pad Size	150um x 150um
	Gross Die	27K ea

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=-250uA	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80V , V_{GS}=0V			-1	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V , V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=-250uA	-1.0	-1.6	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V , I_D=-1A		645	793	m ohm
		V_{GS}=-4.5V , I_D=-0.5A		720	900	m ohm

Notes:

1.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
2.RDS(ON) calculated by SOP-8 Package Type.